Flip-chip bonding of vertical-cavity surface-emitting lasers using laser-induced forward transfer

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This letter reports the use of the Laser-Induced Forward Transfer (LIFT) technique for the fabrication of indium micro-bumps for the flip-chip (FC) bonding of single vertical-cavity surface-emitting laser chips. The FC bonded chips were electrically and optically characterized, and the successful functioning of the devices post-bonding is demonstrated. The die shear and life-time tests carried out on the bonded chips confirmed the mechanical reliability of the LIFT-assisted FC bonded assemblies. © *2014 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4864406]

Flip-chip (FC) assembly of electronic and optoelectronic (OE) components is a key technology in system packaging and integration because of the advantages it offers over the most commonly used wire bonding technique, such as shorter interconnect distance, high packaging density, smaller parasitic resistance, and better device performance.[1] Lead (Pb)-based solder is the most commonly used bump material for FC bonding. Because of the hazardous nature of both the Pb and the flux cleaning solvents, and the high processing temperatures involved, other materials such as Au, Cu, Au-Sn, Ni-Au, conductive adhesives, indium, and indium based alloys are gaining significant interest as Pb-free and fluxless alternatives to solder for FC bonding. In addition, fluxless bonding is an essential requirement for bonding of OE components to avoid contamination of active areas. The most commonly used bumping techniques for these materials are stud bumping, evaporation, electroless/electroplating, and stencil printing.[2] These methods have acquired considerable success over the years for different application areas, but they suffer from drawbacks, such as high processing temperatures, cost, manufacturing time, and above all, most of them lack flexibility.

To mitigate the above-mentioned issues, we employed a laser-based bumping technique called laser-induced-forward-transfer (LIFT) for single-step printing of indium bumps and subsequent FC bonding of single vertical-cavity surface-emitting laser (VCSEL) array chips to these bumps. Indium has excellent cryogenic stability, thermal and electrical conductivity, and low reflow temperature, which makes it a good candidate for FC of optical components.[3] LIFT is an additive and versatile direct-write technique for single-step pattern-definition and material transfer. The basic principle of LIFT involves the focusing of a laser pulse through a transparent substrate (the *carrier*) onto the rear side of a thin film of the material to be printed (the *donor*); this transfers a donor pixel to another substrate (the *receiver*) placed in close proximity (Fig. 1(a)). In the past, LIFT has been used for printing a wide range of materials for various applications.[4–7] Recently, LIFT was also reported for printing conductive inks and pastes for FC bonding applications.[8–10]

LIFT offers several advantages over the existing standard bumping techniques such as, (i) *low temperature processing* which is favourable for many temperature sensitive optical components, (ii) *simplicity* and *versatility* as it enables printing of a wide range of bump materials both in liquid and solid-phase using the same set-up, while for other techniques, the process has to be optimized for each under bump metallization (UBM) and bump metal used, (iii) *cost effectiveness and flexibility* since it is possible to realize bumping and bonding down to chip-scale using LIFT, and finally, (iv) *thinner bumps* can be transferred using LIFT which is desirable to have a smaller separation between the chip and the substrate for the cases requiring an efficient alignment and coupling to optical components.

For the LIFT experiments, indium was used as the donor material. The donor samples were prepared by evaporating 200 nm thick films of indium on top of 4 inch glass substrates. For the receivers, glass substrates (5 cm × 5 cm × 0.07 cm) with lithographically patterned Ni-Au plated bond-pads (80 μm × 80 μm × 4 μm) were used. The donor-receiver assembly was mounted on an X-Y translation stage, and the laser beam was scanned across the sample to transfer indium bumps onto the receiver bond pads. For all the experiments, a Timebandwidth Duetto (355 nm, 12 ps) laser was used, and printing was performed using single laser pulse with the donor placed in contact with the receiver.

Figure 1(b) shows an optical microscope image of a receiver substrate having indium micro-bumps printed onto its contact pads. In this case, six bumps were stacked (printed) on top of each other. The laser fluence used for transferring the metallic bumps was ~270 mJ/cm^2. For stacking, first, an indium bump was LIFTed onto the receiver bond pad, then the donor was moved to a fresh area, and another bump was printed on top of the previously printed one. This was repeated six times to achieve a stack of LIFTed dots with an average height of 1.5 μm and 20 μm diameter. The surface profile and thickness of the printed bumps were measured using an optical profilometer. The adhesion of the bumps was examined using the "scotch tape" test and all the bumps passed this test.

The next step in the process was to bond the OE components to the bumped receiver substrates employing FC bonding. Commercially available VCSEL array chips (1 × 4, 5 Gbps,

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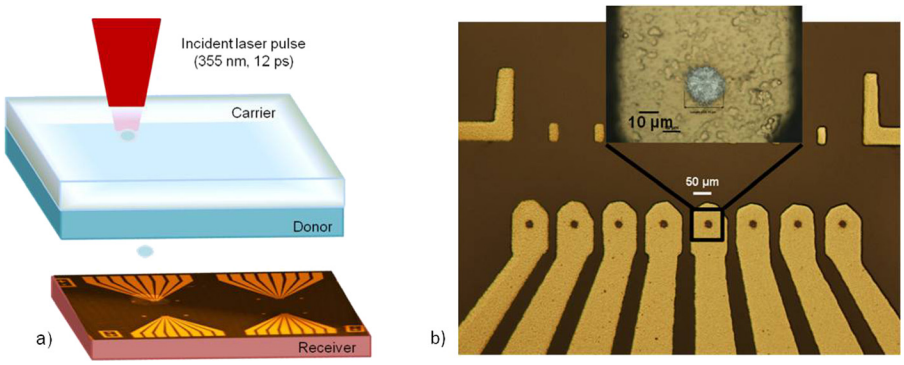

FIG. 1. (a) Schematic of the LIFT technique. (b) Optical image of LIFTed indium bumps onto the receiver bond pads and a magnified image of one of the bumps.

850 nm, size: 1000 μm × 350 μm, thickness: 150 μm) from ULM photonics were chosen as the OE components. A semiautomatic flip-chip bonder (T 320-X) from Tresky was then used to apply thermo-compression bonding of these chips to the conducting bumps, thereby, establishing an electrical and mechanical interconnection between the chips and the substrates. Fig. 2(a) depicts the VCSEL array chip bonded to a bumped receiver substrate with active side facing down. The contact load in the range of 6.25–25 gf/bump-stack was used for bonding the chips and the temperature between the pick-up tool and the chip was set to 190 °C to ensure welding of the chip to the substrate via molten indium bumps (melting point of indium ~157 °C). It is important to mention here that it was difficult to measure the actual temperature at the bonding interface with the present set-up of bonder. The temperature was therefore measured at the chuck that picks up the chip. However, due to non-perfect heat transfer to the bond pads on the other side of the chip, the actual temperature at the bonding interface is lower than 190 °C. Figure 2(b) shows the cross-section of an interconnection realized between the VCSEL chip pad and the substrate after FC bonding using LIFTed indium bump.

To verify the functionality of the FC bonded VCSEL arrays, their electrical and optical characteristics were measured. Fig. 3(a) depicts the typical light-current-voltage (LIV) curves recorded for the bonded VCSELs (solid curve). Similar behaviour was observed for all the VCSEL chips bonded using different contact loads. The measured optical power matched well with that from the unbonded VCSEL chips, thereby illustrating the successful functioning of all the bonded devices. To test the reproducibility of the method, more than 15 VCSEL chips were prepared and characterized and all of them demonstrated similar characteristics. The current voltage (I–V) curves were measured for the VCSELs before and after FC bonding. The recorded curves for a bare die and bonded using different pressures are shown in Fig. 3(b). There is almost no difference between the I–V curves of the bonded chips and those of the bare die for all the cases, indicating negligible additional resistance of the bumps.

To evaluate the mechanical ruggedness of the bonded assemblies, die shear tests were performed using a Dage 4000 series machine. During the tests, a shear force was applied to the assembly up to the point where bonded chips were detached from the substrate. The chips completely separated from the contact pads on applying an average force of ~34.3 gf, which corresponds to a force of ~4.3 gf per bond site. The bumps fractured in the middle during the tests, which is the optimum case, indicating good adhesion of the bumps to the contact/bond pads both on the substrate and on the chips.

In order to increase reliability of the bonded VCSEL assembly, a single component UV curable and optically transparent adhesive NOA 86 from Norland was used for encapsulation. The adhesive was dispensed around the edges of the bonded chips using a syringe needle and cured for ~30 s using an Omnicure 1000 UV lamp. It should be mentioned that because of its low viscosity, the adhesive to some extent underfilled the small space between the chip and the substrate due to capillary action. The LIV curves recorded for the bonded VCSELs before and after encapsulation are shown in Fig. 2(a) (dotted curve corresponds to an encapsulated assembly). Clearly, the encapsulation did not affect the interconnection and the functioning of the VCSEL arrays. There was no difference in the I–V curves of the chips before and after encapsulation. However, a slight variation in the optical power was observed after encapsulation that is attributed to the measurement errors. The die shear tests conducted on the encapsulated assemblies resulted in breaking

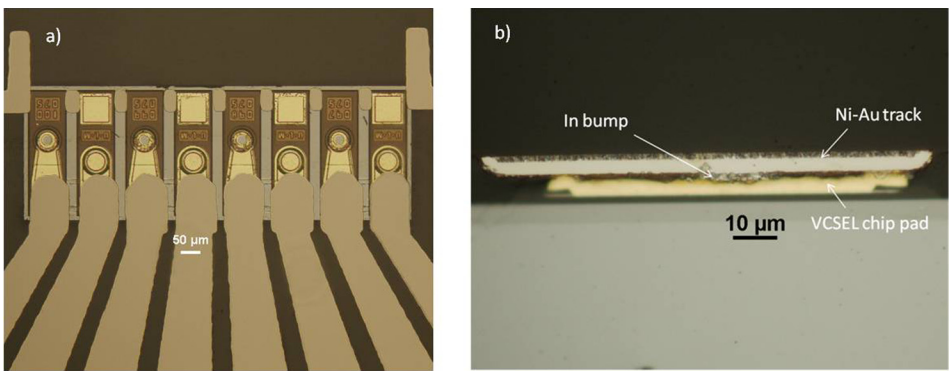

FIG. 2. (a) Optical micrograph of a FC bonded VCSEL array chip as viewed from the backside of the receiver substrate. (b) Cross-section of an interconnection between the VCSEL chip and substrate via indium bump.

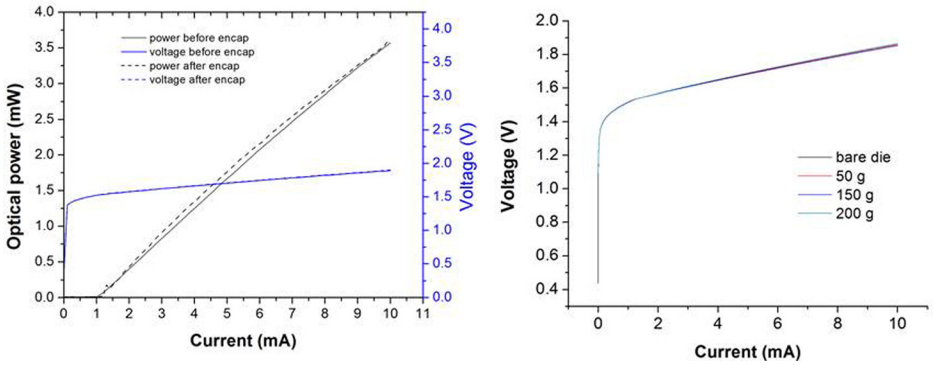

FIG. 3. (a) Typical LIV curves recorded for the LIFT-assisted flip-chip bonded VCSELs before (solid) and after encapsulation (dotted); (b) I–V curves recorded for unbonded (bare die) chips and chips bonded using different bonding pressures.

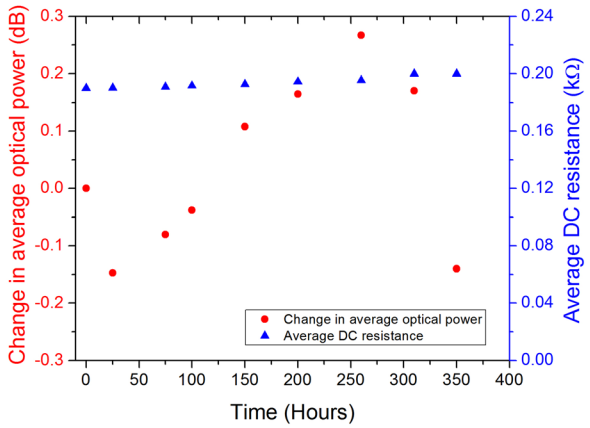

FIG. 4. Variation in average optical power and average DC resistance with the ageing time.

and damaging of the chips without detaching them from the substrate.

To estimate the life-time of the bonded and encapsulated chips, a standard 8585 accelerated ageing test was performed on 3 different samples (12 VCSELs in total). The test samples were kept in a climate chamber under controlled temperature (85 °C) and humidity (85% relative humidity (RH)) conditions for a total of 350 h. The electrical and optical characteristics for each of the VCSELs were monitored at periodic intervals. Both the optical power and DC resistance were recorded for a driving current of 10 mA. The change in average optical power (difference in the optical power before and after ageing test, expressed in dB) and the average DC resistance obtained from the measurements are plotted in Fig. 4. For the optical power, the variation was <0.3 dB, whereas virtually no change was measured for the DC resistance. This clearly shows a minimal degradation in the performance of the test VCSELs due to any probable moisture penetration at elevated temperature even after a total of 350 h at 85 °C/85% RH.

In conclusion, LIFT-assisted thermo-compression flip-chip bonding of single VCSEL chips was demonstrated using indium bumps. The optical, electrical, and mechanical reliability of the bonded devices was evaluated. The results obtained show the great potential of the LIFT technique for interconnect technology, especially for applications that require single chip bumping, high accuracy, and fine pitch for high-density flip-chip interconnections.

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