

COMPOSE (Characterisation, Optimisation and Modelling of Power Semiconductor devices)

1. Introduction

The continuous shrinking of standard CMOS technologies is driven by the increased digital complexity required by new applications. For applications requiring real power capabilities (>100 W), power transistors need to be made as discrete components. The driving circuitry of the power transistor has to be done on a separate chip, leading to expensive multi-chip solutions. However, there is also an increased interest from the market for so-called Power Integrated Circuits, which integrate power handling capabilities and digital logic on the same chip.

It is obvious that the integration of power handling capabilities in a sub-micron CMOS technology will have to solve the paradigm of combining high voltages and high currents needed to drive e.g. a motor, with the low voltage and low current requirements of digital CMOS. This is the field of the so-called smart power technologies. In the development of such technologies, one starts with a standard CMOS core (e.g. 0.35 μm CMOS logic) and adds the necessary process layers in order to cope with the higher voltages. To handle the necessary current levels, special attention has to be paid to the distribution of the currents in the device. Special layout optimisation towards current and heat distribution has to be taken into account. Also one has to choose appropriate bonding techniques and power packages to minimize the heating of the chip by optimising the heat dissipation. In addition, alternative device concepts for handling high currents need to be investigated. Special devices need to be simulated with TCAD, and then integrated in the smart power process flow.

Of equal importance is the correct characterisation of the power devices and their subsequent qualification. New characterisation and measurement techniques have to be developed and applied. The standard CMOS characterisation techniques are not applicable as power devices operate under much different conditions (e.g. characterisation of lattice heating, heat distribution, switching of inductive, capacitive or resistive loads, ...). It is the goal to develop a suitable characterisation procedure for integrated power devices. Also some special equipment needs to be developed and tested such as a wafer level energy capability system to measure the energy capability of the devices under different loads. Another special measurement setup to be verified is for accurately measuring degradation characteristics at low temperatures (specification for the automotive industry is -40°C). Hot carrier measurements have to be done both under DC as well as under AC conditions.

2. Objective

The overall objective of the proposed project is to perform an in-depth study on the power capabilities of the existing smart power technologies of the Industrial Partner (AMI Semiconductor), this in order to extend the use of these technologies to the medium power range (up to 10A). A strong motivation for investigation in this field is the large market segment for motor drivers which require current levels between 5 and 10A. Important aspects to be covered are:

- Development of characterisation techniques for integrated power devices, which differs largely from the standard CMOS characterisation techniques. Especially all the issues related to lattice heating and the subsequent degradation mechanisms have to be investigated in detail.
- The integrated power devices will have to be modelled. Especially the modelling of the thermal resistance as a function of the area and the width of the transistors is mandatory. In order to improve the understanding of the behaviour of such devices under power pulse conditions, 3 dimensional simulations will have to be run, as thermal problems are essentially 3D.
- New device concepts will have to be evaluated. These devices will be integrated in the smart power technologies of AMIS (I2T and I3T) and their current capability will be evaluated by using above mentioned characterisation techniques.

- In order to improve the heat dissipation, different power packages will be evaluated. In addition the effect of special layout techniques and bonding patterns (direct bonding) will be investigated. The addition of a thick top copper metal to redistribute the heat in the power device will be studied.

3. Contribution of the TFCG group

The TFCG group will carry out TCAD process and device simulations to investigate the feasibility of integrating novel high-voltage power devices in the I3T technology of AMIS. Strong emphasis will be put on the IGBT (Insulated Gate Bipolar Transistor), but other interesting structures such as the SCR (Silicon Controlled Rectifier) or the LILET (Lateral Inversion Layer Emitter Transistor) might be taken into consideration as well.