

## 3D stacking of ultrathin chips and chip packages

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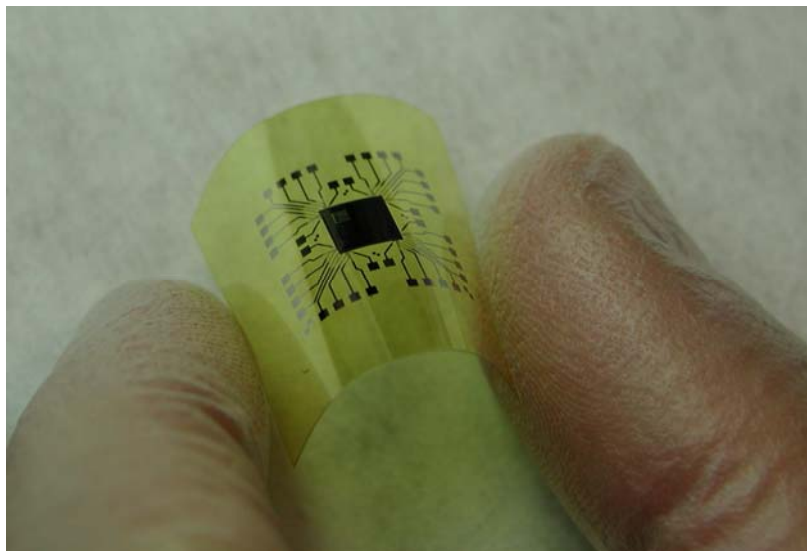
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### Imec strategy :

The proposed PhD research fits in the domain of flexible and stretchable electronics, and especially in that of wafer and chip thinning and packaging / embedding of ultrathin chips.

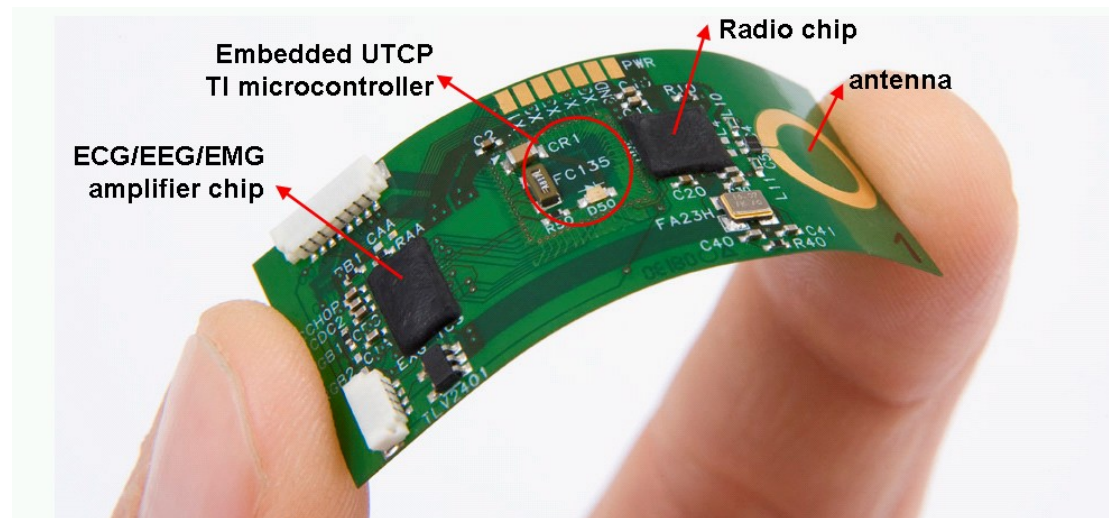
### Short description of the PhD subject :

In the frame of the EC funded project SHIFT (Smart High Integration Flex Technologies) technology has been developed for an ultrathin chip package (UTCP). In this technology a 25 $\mu$ m thin Si chip is embedded in an organic carrier, consisting of cured spin-on polyimide layers. Contacts of the chip to the outside world are realised using laser drilling or RIE (reactive ion etching) through the polyimide to the chip pads and thin film interconnection metallisation. The result is a package of 60 $\mu$ m thickness only, which can be bent (including the chip). The figure below shows a realised UTCP. The technology is the subject of a recent common IMEC – UGent patent application<sup>1</sup>.



This type of package can be used for embedding in the inner layers of a printed circuit board (PCB) or a flex interconnection substrate. Thus the third dimension of the substrate is used, and very compact circuits are obtained. The figure below shows a wireless flexible ECG (electrocardiogram) measurement module, in which one of the three chips (a Texas Instruments

(TI) Microcontroller) is packaged as an UTCP and subsequently is embedded in the flex substrate during the flex production process. Below and above the embedded UTCP passive components are assembled.



The goal of the proposed PhD work is to go one step further and to develop technology for an ultracompact package of a number of chips, based on the stacking of ultrathin chips.

At this moment stacking of chips is realised using D2D (die-to-die) and D2W (die-to-wafer) bonding, followed by wire-bonding. The stacking of a multitude of dies, combined with an increase of the number of interconnections (involving wire bonds with long wires, which bridge several “levels” of the stack), result in severe yield and reliability problems. On the other hand the demand from industry for stacked chip packages is very strong, e.g. in mobile phones where ultracompact packaging and assembly is of utmost importance.

To solve the problems, that current technologies for stacked chips using wirebonding have, a number of groups perform research on the realisation of interconnections through the chips (“through silicon via” – TSV technology). This is however an expensive technology and cannot cope with the case that different types of chips have to be packaged in one “hybrid” or “heterogeneous” package. Also PoP (“package on package”) is a proposed solution, but in this case RF performance and compactness is not as good as the one obtained in the TSV technology.

It is believed that stacking of UTCPs will combine the advantages of both PoP and TSV technologies: cost effectiveness, compactness, RF capability, flexibility in combining chips from various origins and with different designs and technologies.

The PhD work will investigate feasibility and reliability of different ways of ultrathin chip stacking. Precise ideas on possible process flows exist at TFCG, but can not be disclosed in this document because of IP (Intellectual Property) reasons. When developing the technology, one has to take into account

following boundary conditions in view of the current development of semiconductor technology:

- Increasing interconnection density
- Electrical signal integrity, especially RF behaviour
- Thermal management
- Reliability of the package and assembly on a standard Printed Circuit Board (PCB)

Therefore, besides the stacking of chips, also additional structures like decoupling capacitors, matched impedance lines, heat spreading structures, etc. will be embedded in the stack.

Furthermore the package will be assembled on, or embedded in a standard PCB and the reliability of this assembly will be studied.

The work will in a first phase make use of interconnection test chips for the development of the technology. Towards the end of the PhD also one or more functional demonstrators for validation of the technology will be realised. A first possibility is a stack of memory chips (e.g. Flash), in order to obtain an ultracompact memory module with very high capacity per cubic mm. At this moment it is forecasted to be possible to integrate 15 chips in a stack of 1mm thickness. A second demonstrator possibility is the design and construction of a stacked chip module, including a physiological sensor signal measurement chip, a microcontroller and an RF communication chip for wearable sensors and electronics applications, demonstrating the capability for heterogeneous chip assembly and RF capability of the technology. In this way an extremely compact ECG measurement module, with the same functionality as the one shown above, can be produced. Finally CMST is a partner in the EC funded project "TIPS" (Thin Interconnected Package Stacks), in which a.o. the Danish company Oticon (producer of hearing aids) wants to use this technology in its products.

In the frame of this PhD the work to be performed will be technology development (processes and reliability assessment for the fabrication of UTCP stacks), as well as electronic design and testing (functional demonstrator design, fabrication and testing).

On the subject a CMST co-worker has performed already 1 year of work, which can be included in the PhD. The three available additional grant years will be sufficient to finish the PhD.

Start of the grant: possible from July 1, 2009, on, preferably September 1, 2009, at the latest.

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<sup>1</sup> J. Vanfleteren, W. Christiaens, "Method for Embedding Dies", US patent app., Appl. Serial No. 11/602,733, filed November 21, 2006.